## **Assistant Professor**



**Education:** M.Tech

Email: saidulur@rgukt.ac.in / saidulurapolu@gmail.com Phone: +91 -9700841353 Mr. Rapolu saidulu has joined the institute in 2016.

## **WORK EXPERIENCE**

#### • Assistant Professor :

 Working as an Assistant Professor, Rajiv Gandhi University of Knowledge Technologies(RGUKT) Basar from AUGUST 2016 - till date (5 years)

#### Assistant Professor:

 Worked as an Assistant Professor, Sri Indu Engineering College (SIEC)–HYD from April 2015 - AUG 2016

## **RESEARCH PUBLICATIONS (03)**

## **International Journals (02)**

- R. Saidulu, A. Sai Chaitanya; "Pre-encoded multiplier based on non-redundant radix-4 signed digit encoding"; Anveshana's International Journal of Research in Engineering and Applied Sciences, Volume 03. Issue 06, pp. 60-65, 2018, ISSN 2455-6300.
- 2. A. Sai Chaitanya, **R. Saidulu**; Comparative study of dsp architectures for wireless sensor nodes"; **Anveshana's International Journal of Research in Engineering and Applied Sciences**, Volume 03, Issue 06, pp.65-71, 2018; **ISSN 2455-6300**

## **International Conferences (01)**

 Surender M, Chandra Shekar K, Ravikanth K, Saidulu R. "Automatic Identification of Bird Species from the Image Through the Approaches of Segmentation," in the Technical Session Network Security/Image Processing of the 6th International Conference on Innovations in Computer Science & Engineering(ICICSE-2018), held during 17<sup>th</sup>-18<sup>th</sup> August, 2018.

## **PROJECTS SUPERVISION (07)**

- 1. Low power and Fast Full Adder By Exploring New XOR and XNOR Gates.(Bachelor's)
- 2. CMOS Telescope Cascode Operational Amplifier (Bachelor's)
- **3.** Graph-Based Transistor Network Generation Method For Supergate design. (Bachelor's)
- **4.** Data Encryption Using AES by Verilog. (Bachelor's)
- 5. The Mesochronous Dual-Clock FIFO Buffer. (Bachelor's)
- **6.** Design of FPGA based 32-bit floating point arithmetic unit. (Bachelor's)
- 7. Design, Implementaion and comparision of 8-bit Vedic Multiplier Using Multiplexers and Logic Gates.(Bachelor's)

- Low-Power VLSI Circuits.
- Nano Devices
- MEMS and Sensors
- Analog and Mixed Mode systems

## **SUBJECTS TAUGHT**

## **B.Tech:**

- Analog Electronic Circuits (E2-EC2201)
- Analog communications(E3-EC3101)
- Digital Electronic Circuits (E2-EC2202)
- Basic Electrical and Electronics Engineering (E1 1001/2001)
- Basic Electrical Engineering (E1-EE1002 & E1-EE1203)
- Signals & Systems (E2-EC2103)
- Digital signal processing.
- VLSI Engineering.

## WORKSHOPS / SHORT TERM COURSES (07)

- One-week faculty development programon "FUTURE NANO ELECTRONIC DEVICES & CIRCUITS" organized by Department of Electronics & Communication Engineering, MGIT, Hyderabad from 6<sup>th</sup> to 10<sup>th</sup> July 2020.
- **TEQIP-III** sponsored Five Day Continuing Education Program on "5G **TECHNOLOGIES**" organized by the Department of Electronics and Communication Engineering, National Institute of Technology, Warangal from 14<sup>th</sup> to 18<sup>th</sup> May 2018.
- **TEQIP-II** sponsored six Day Continuing Education Program on "**INTERNET OF THINGS(IOT)**" organized by the Department of Electronics and Communication Engineering, National Institute of Technology, Warangal from February 27<sup>th</sup> to 04<sup>th</sup> March 2017.
- One-weekfaculty development program on "Recent Trends in Control system Engineering" Organized by Department of Electrical Engineering, NIT Patna under the banner of Electronics And ICT Academy, NIT Patna, held From 22<sup>nd</sup> to 28<sup>th</sup> June,2020
- One-weekfaculty development program on "Recent Trends in VLSI Design"
  Organized by Department of Electronics and Communication Engineering, Lakshmi
  Narain College of Technology & Science, Bhopal MP from 22<sup>nd</sup> to 26<sup>th</sup> June, 2020
- Short-term practical training and evaluations for "Instructional Excellence in Intelligent Systems under the Intel College Excellence Program" conducted by Rajiv Gandhi University of Knowledge technologies, Basar, From 1<sup>7th</sup> -2<sup>0th</sup> Sept, 2016.
- One-Day workshop on "**Designing Ternary Logic Gates using Furtheristic Nano Devices**"organized by Department of Electronics and Communication Engineering, Vidya Jyothi Institute of Technology, Hyderabad on 20<sup>th</sup> June 2020.

# Department Level Faculty in-charge/coordinator

- Incharge for General administration of Department level activities.(Mar2021-Till Date)
- Time table incharge (Mar2021-Till Date), Department of ECE, RGUKT, Basar.
- Sports Coordinator (2017-2018), Department of ECE, RGUKT, Basar.
- NAAC Coordinator (Jan 2021- Mar 2021), Department of ECE, RGUKT, Basar.
- Faculty Incharge for Analog Electronic Circuits Lab (Jan2021-Till Date), Department of ECE, RGUKT, Basar.
- Qualified in National Eligibility Test (NET)-2018.
- Qualified in GATE 2014.

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