



Assistant Professor

Education: Ph.D (Pursuing) in OU HYD

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Mr. **Chintam Shravan** has joined the institute in 2016.

Social Media:

<https://www.youtube.com/c/SHRAVANCHINTAM>

WORK EXPERIENCE

- **Assistant Professor :**
 - Working as an Assistant Professor, Rajiv Gandhi University of Knowledge Technologies(RGUKT) Basar from **AUGUST 2016 - till date (5 years)**
- **Assistant Professor:**
 - Worked as an Assistant Professor, Matrusri Engineering College (MEC)–HYD from **July 2015 - AUG 2016**

RESEARCH PUBLICATIONS (05)

International Journals (02)

1. **Ch. Shravan, B. Venkanna;** “Bank Locker Security System with password and Intruder Alarm”; **International Journal of Recent Developments in Science & Technology**, Volume 03. Issue 01, pp. 72-77, 2019, **ISSN 2581-4575**.
2. **B. Venkanna, Ch. Shravan;** “ A hybrid Encryption Protocol based on AES and RSA for Implementation in Cognitive Radio Networks”; **Anveshana’s International Journal of Research in Engineering and Applied Sciences**, Volume 02, Issue 07, pp.80-85, 2017; **ISSN 2455-6300**

International Conferences (03)

1. Shravan, CH.; Pavan Kumar, CH.; Sivani, K., "A novel approach for power reduction in asynchronous circuits by using AFPT," *Wireless and Optical Communications Networks (WOCN), 2014 Eleventh International Conference on* , vol., no., pp.1,7, 11-13 Sept. 2014, doi: 10.1109/WOCN.2014.6923091.
2. Shravan, Ch.; Pavan Kumar Ch.; Sivani, K., "A novel approach for power-gating technique with Improved Efficient Charge Recovery Logic," *Smart Electric Grid (ISEG), 2014 International Conference on* , vol., no., pp.1,8, 19-20 Sept. 2014 doi: 10.1109/ISEG.2014.7005583.
3. O. Anjaneyulu, CH. Shravan, A. Veena, C. V. Reddy, “ **Self Driven Pass Transistor based Low Power Pulse Triggered Flip-Flop Design (LPPF)** ” *IEEE International Conference on Signal Processing and Communication Engineering Systems (SPACES)*, 2nd& 3rd January, 2015, KL University, Vijayawada, Andhra Pradesh, India.

GOOGLE SCHOLAR:

<https://scholar.google.co.in/citations?hl=en&user=TVA9nroAAAAJ>

PROJECTS

- **Master's Thesis:** A novel Approach for Power reduction in Asynchronous circuits by using AFPL
 - **Guide:**
 1. Dr. K. Sivani, KITS, WGL, India.

Description:An AFPL developed by Improved Efficient Charge Recovery Logic (IECRL), which gives logic function to the next succeeding stage. In the AFPL circuit, IECRL gates attains power from hand shake controller and become active only when executing required calculations. In active mode the leakage currents are reduced by providing high resistance path through the NMOS transistor in pull-up network. In in-active mode IECRL gates are not taken any amount of power, this gives insignificant leakage power dissipation. Its maximum power saving against ECRL is up to 89.35%. In AFPL circuit handshake controller used to provide power to the IECRL gate and which handles the hand shaking with the neighboring stages. In the AFPL circuit PCR mechanism is used to transfer the charge of discharging phase of IECRL gate to evaluate phase of the another IECRL gate, to reduce the energy dissipation. Early discharging of IECRL gate can be achieved by using modified C-element called C*-element.

PROJECTS SUPERVISION (07)

1. Current based Data Retention Time (IDRT) characterization methodology for Gain-Cell Embedded DRAM, as an alternative of existing SRAM Memory cell.(Bachelor's)
2. Improving Energy-Efficiency in Dynamic Memories Through Retention Failure Detection. (Bachelor's)
3. Improving Data Retention Time (DRT) failures in GC-eDRAM structure. (Bachelor's)
4. A 3-Transistor nMOS-only logic compatible Gain-Cell Embedded DRAM for alternative SRAM's at 1000 mV in 45-nm FD-SOI. (Bachelor's)
5. Improved Gain-Cell Embedded DRAM: Timing; Availability, bandwidth and area improvement. (Bachelor's)
6. Efficient VLSI Implementation of a Sequential Finite Field Multiplier Using Reordered Normal Basis in Domino Logic. (Bachelor's)
7. Study on the Anti-Theft Technology of Museum Cultural Relics based on Internet of Things (IoT). (Bachelor's)

RESEARCH INTERESTS

- Memories
- Low-Power VLSI Design for IoT applications
- Gain-Cell Embedded DRAM's
- Magneto-Resistive Random-Access Memory (MRAM's)
- Ferro-Electric Random-Access Memory (FRAM's)
- Fin-FET based GC-eDRAM's

SUBJECTS TAUGHT

M.Tech:

- Mixed SignalCircuit Design (MSCD)

B.Tech:

- ESIOT (E4-EC4403)
- Analog Electronic Circuits (E2-EC2201)
- RFMW (E3-EC3102)
- Digital Electronic Circuits (E2-EC2202 & E1-EC1101)
- Linear Control System Engineering (E2-EE2202)
- Electrical and Electronic Measurement & Instrumentation (E4-EC4426)
- Digital Communication (E3-EC3201)
- Basic Electrical Engineering (E1-EE1002 & E1-EE1203)
- Signals & Systems (E2-EC2103)

WORKSHOPS / SHORT TERM COURSES (10)

- One-week faculty development program on **“FUTURE NANO ELECTRONIC DEVICES & CIRCUITS”** organized by Department of Electronics & Communication Engineering, MGIT, Hyderabad from 6th to 10th July 2020.
- **TEQIP-III** sponsored Five Day Continuing Education Program on **“5G TECHNOLOGIES”** organized by the Department of Electronics and Communication Engineering, National Institute of Technology, Warangal from 14th to 18th May 2018.
- One-week **GIAN (Global Initiative of Academic Networks)** course on **“ADVANCED CMOS CLOCK GENERATION CIRCUITS” (Course Code:171036D01)** organized by the Department of Electronics and Communication Engineering National Institute of Technology Warangal during December 25 – 29, 2017. Foreign Faculty/Expert: Dr. Pavan Kumar Hanumolu.
- Short-term course on **“ENGINEERING RESEARCH METHODOLOGY (ERM-2017)”** held during 11-14 December, 2017 in the department of Mechanical Engineering, University College Engineering (Autonomous), Osmania University, Hyderabad, Telangana state-500007.
- One-week faculty development program on **“Real Time Embedded Systems and IoT, Its Applications”** Organized by the E & ICT Academy, National Institute of Technology, Warangal, at the Department of ECE, Vardhman College of Engineering (Autonomous), Hyderabad from 5th -10th December, 2016. (Sponsored by Meity, Govt of India)
- Short-term practical training and evaluations for **“Instructional Excellence in Intelligent Systems under the Intel College Excellence Program”** conducted by Rajiv Gandhi University of Knowledge technologies, Basar, From 13th -16th Sept, 2016.
- One-Day workshop on **“National Programme on technology Enhanced learning (NPTEL)”** organized IIT Madras on 9th July, 2016 at Vardhman College of Engineering, Hyderabad.
- 12-week Short term course on **“Basic Electrical Circuits”** which is organized by IIT Madras through National Programme on Technology Enhanced Learning (NPTEL).
- 12-week Short term course on **“Digital Circuits & Systems”** which is organized by IIT Madras through National Programme on Technology Enhanced Learning (NPTEL).
- 8-week Short term course on **“Introduction to Electro-Magnetic Theory”** which is organized by IIT Kanpur through National Programme on Technology Enhanced Learning (NPTEL).

ADDITIONAL RESPONSIBILITIES & ACADEMIC ACHIEVEMENTS

University Level

- Member, APC advisory (2021 – Till Date), Department of ECE, RGUKT-Basar
- Member, NAAC Committee (17-12-2019 to Till Date), RGUKT, Basar.
- Member, Cultural Committee(07-02-2018 to 30-07-2018), RGUKT, Basar.

Department Level Faculty in-charge/coordinator

- Cultural Coordinator (2017-2018), Department of ECE, RGUKT, Basar.
- Library Coordinator (2018 - Feb 2021), Department of ECE, RGUKT, Basar.
- NAAC Coordinator (2017-Till Date), Department of ECE, RGUKT, Basar.
- NBA Coordinator (2021- Till date), Department of ECE, RGUKT, Basar.
- Micro Wave Engineering Lab (2017-Till Date), Department of ECE, RGUKT, Basar.

RESOURCE LECTURES/CONFERENCE PRESENTATIONS (04)

S.No	Name of the event/workshop	Title of the Lecture	Institute/ Industry	Date
1	WOCN-2014 conference	A novel approach for power reduction in asynchronous circuits by using AFPT	KLU, Vijayawada	11 th to 13 th Sept., 2014
2	ISEG-2014 conference	A novel approach for power-gating technique with Improved Efficient Charge Recovery Logic.	KLU, Vijayawada	19 th to 20 th Sept, 2014
3	SPACES-2015 conference	Self-Driven Pass Transistor based Low Power Pulse Triggered Flip-Flop Design (LPPF)	KLU, Vijayawada	2 nd to 3 rd Jan, 2015
4	National Seminar on RTES-2015	Fine Grained Power gating for leakage and short circuit power reduction by using Asynchronous logic.	MGU, Nalgonda	27 th March, 2015